

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**In re U.S. Patent Application of -**  
**SAITO et al.**  
**Application Number: To be Assigned**  
**Filed: Concurrently Herewith**  
**For: SEMICONDUCTOR DEVICE**  
**ATTORNEY DOCKET NO. HITA.0501**

**Honorable Assistant Commissioner  
for Patents  
Washington, D.C. 20231**

## **INFORMATION DISCLOSURE STATEMENT**

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, this Information Disclosure Statement is submitted in the above-identified patent application. A listing of documents to be published on the face of any patent granted from this application is submitted herewith on Form PTO-1449. Any other documents or information submitted for consideration by the Examiner are listed in this paper. A copy of each U.S. and foreign patent, or each publication or portion thereof listed or herein identified, is submitted herewith.

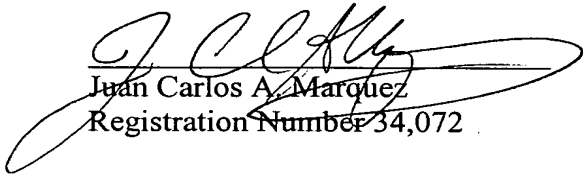
This Information Disclosure Statement is submitted with the initial filing of the application. Accordingly, no fee is due or payable at this time.

The Examiner is requested to acknowledge consideration of the information provided in this paper in accordance with prescribed procedures.

Please charge any additional fees or credit any overpayments in connection with this paper to Deposit Account No. 08-1480.

Respectfully submitted,

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	APPLICANT SAITO et al	
	FILING DATE Concurrently herewith	GROUP

**U.S. Patent Documents**

Examiner Initial	DOCUMENT NUMBER	DATE	NAME	CLA SS	SUBC LASS	FILING DATE

**Foreign Patent Documents**

Examiner Initial	DOCUMENT NUMBER	FILING DATE	COUNTRY	CLASS	SUB- CLA SS	TRANSLATION	
						YES	NO
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**Other Documents (Including Author, Title, Date Pertinent Pages, Etc.)**

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		Patrick P. Gelsinger, "Microprocessors for the New Millennium: Challenges, Opportunities, and New Frontiers", 2001 IEEE International Solid-State Circuits Conference, 10 pages
		D.A. Buchanan et al. "80 nm Poly-silicon Gated n-FETs with Ultra-Thin Al <sub>2</sub> O <sub>3</sub> Gate Dielectric for ULSI Applications", IEEE (2000), 4 pages
		K. Torii et al., "Fixed Charge-Induced Mobility Degradation and its Recovery in MISFET's with Al <sub>2</sub> O <sub>3</sub> Gate Dielectric", IWGI 2001, Tokyo, pp. 230-232
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		K. Rim et al., "Mobility Enhancement in Strained Si NMOSFETs with HfO <sub>2</sub> Gate Dielectrics", IEEE, 2002 Symposium on VLSI Technology Digest of Technical Papers, 2 pages
		Kunihiro Suzuki et al., "Scaling Theory for Double-Gate SOI MOSFET's", IEEE Transactions on Electron Devices, Vol. 40, No. 12, December 1993, pp. 2326-2329
		International Technology Roadmap for Semiconductors, 2001 Edition, "Front End Processes", pp. 1-44
EXAMINER		DATE CONSIDERED

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